CLAIMS

What is claimed is:

1. A microprocessor comprising:

a plurality of dynamic pipeline stages including at least one predicated instruction wherein the predicated instruction includes a plurality of guarding predicates;

a register renaming unit;

a reorder buffer;

a plurality of execution units;

a plurality of reservation stations wherein the register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the plurality of dynamic pipeline stages; and

an augmented register alias table.

2. The microprocessor of Claim 1, wherein the register renaming unit renames each one of a plurality of source registers of the pipeline instruction and renames a destination register to a new physical register.

3. The microprocessor of Claim 2, wherein the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers.

4. The microprocessor of Claim 3, wherein each one of a plurality of select-μops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier.

5. The microprocessor of Claim 4, wherein the plurality of source operands comprises a first source operand and a plurality of secondary source operands.

6. The microprocessor of Claim 5, wherein the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available.

7. The microprocessor of Claim 5, wherein each one of the plurality of secondary source operands includes a plurality of status bits and a physical register identifier.

8. The microprocessor of Claim 7, wherein each one of the plurality status bits has a ready bit and a committed bit.

9. A method of processing predicated instructions comprising:

receiving a plurality of predicated instructions assigned to a common defined destination register and wherein at least one of the plurality of predicated instructions is out of order in an dynamic pipeline;

renaming the destination register for each one of the plurality of predicated instructions;

assigning the corresponding renamed destination register for each one of the plurality of predicated instructions with a corresponding predicate register to corresponding ones of the a plurality of source operands of a select-μop;

determining a valid predicate in the source operands of the select-μop;

selecting the register corresponding to the select-μop that corresponds to the valid predicate;

transferring the data in the selected register to the destination register; and

executing a consumer instruction wherein the consumer instruction uses the data from the destination register of the corresponding select-μop.

10. The method of Claim 9, wherein the each one of the plurality of select-μops has a plurality of source operands wherein each one of the plurality of source operands corresponds to a physical register identifier.

11. The method of Claim 10, wherein the plurality of source operands comprises a first source operand and a plurality of secondary source operands.

12. The method of Claim 11, wherein the first source operand includes a default physical register identifier, wherein the default physical register is always valid and available.

13. The method of Claim 11, wherein each one of the plurality of secondary source operands includes a plurality of status bits and a physical register identifier.

14. A computer system comprising:

a processor, wherein the processor includes:

a plurality of dynamic pipeline stages including at least one predicated instruction wherein the predicated instruction includes a plurality of guarding predicates;

a register renaming unit;

a reorder buffer;

a plurality of execution units;

a plurality of reservation stations wherein the register renaming unit, the reorder buffer, the plurality of execution units and the plurality of reservation stations are coupled to at least one of the plurality of dynamic pipeline stages; and

an augmented register alias table;

a system bus;

a computer memory system;

an input/output device;

wherein the system bus is coupled to the processor, the computer memory system and the input/output device.

15. The computer of Claim 14 wherein, the augmented register alias table includes a plurality of lines, and wherein each one of the plurality of lines includes a plurality of renamed destination registers.

16. The computer of Claim 15 wherein, the register renaming unit renames each one of the plurality of source registers of the pipeline instruction and renames the destination register to a new physical register.